REMARKS

Entry of the foregoing, re-examination and reconsideration of the subject matter identified in caption, as amended, pursuant to and consistent with 37 C.F.R. §1.114, and in light of the remarks which follow are respectfully requested.

By the amendments, non-elected claim 1 has been revised to depend from claim 13 of the elected invention and for consistency with amended claim 13. In addition, independent claims 13, 24 and 27 have been amended by pointing out that the dielectric layer is planar and that the patterned metal layer is disposed directly on the dielectric layer. Claims 13 and 24 have further been amended by deleting the previously added feature directed to the patterned metal pad, and by the addition of an optical component in the etched pit.

Turning now to the rejections, claims 13-29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ayliffe et al (U.S. Patent No. 5,522,000). Claims 13-29 also stand rejected under 35 U.S.C. §103(a) as being obvious over Ayliffe et al. The claims as now presented cannot properly be rejected on these grounds.

The present invention relates to etched optoelectronic apparatus. The apparatus as set forth, for example, in independent claim 13 comprises: a) a semiconductor substrate having an etched pit with semiconductor sidewalls; b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls; c) a patterned metal layer disposed directly on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls; and d) an optical component in the etched pit.

Ayliffe et al discloses a method of making a multilayered printed circuit on a single crystal substrate for mounting thereon at least one electro-optic transducer and at least one optical component. The printed circuit has a plurality of electrical conductors. (Col. 2, lines 1-5).

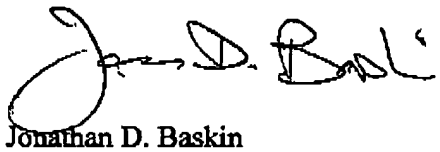
Ayliffe et al does not disclose or suggest each feature of the present invention. For example, Ayliffe et al does not disclose or fairly suggest an etched optoelectronic apparatus having a dielectric layer disposed on a semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls aligned with the semiconductor sidewalls, and a patterned metal layer disposed directly on the planar dielectric layer, as now claimed in independent claims 13, 24 and 27. Quite to the contrary, the metal pads 16b of Ayliffe et al sit directly on a dielectric layer 14 which is non-planar. In this regard, Ayliffe et al discloses that

prior to depositing the dielectric layer 14, a passivation layer 11 is deposited and a patterned interconnect layer 13 is formed on layer 11. The dielectric layer 14 is formed over the patterned interconnect layer 13, thereby rendering the dielectric layer 14 non-planar. Ayliffe et al requires formation of the interconnect layer 13, and there is no disclosure or suggestion in that document to form anything other than a multilayered printed circuit having such a structure. Thus, persons skilled in the art would not have modified the Ayliffe et al multilayered printed circuit to arrive at applicants' invention. Accordingly, withdrawal of this rejection is respectfully requested.

From the foregoing, further and favorable action in the form of a Notice of Allowance is believed to be next in order, and such action is earnestly solicited.

If there are any questions concerning this paper or the application in general, the Examiner is invited to telephone the undersigned at his earliest convenience.

Respectfully submitted,



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MARKED-UP VERSION SHOWING AMENDMENTS

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A method for fabricating [accurately located etched features on a semiconductor substrate,] the etched optoelectronic apparatus of claim 1, comprising the steps of:

a) providing a semiconductor substrate with a top surface and a planar dielectric layer on the top surface;

b) forming a patterned metal layer on the dielectric layer, wherein the patterned metal layer has a metal edge;

c) forming a patterned resist layer on the dielectric layer and patterned metal layer, wherein the resist layer has a resist edge that is located on top of the metal layer such that the dielectric layer has an exposed area defined by the metal edge;

d) etching away the dielectric layer from the exposed area;

g) etching the semiconductor substrate where the dielectric layer is etched away in step (d), thereby forming a pit; and

h) placing an optical element into the pit.

13. (Twice Amended) An etched optoelectronic apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;

b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls;

c) a patterned metal layer disposed directly on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls; and

d) an optical component in the etched pit. [a patterned metal pad disposed on the dielectric layer;

e) solder disposed on the patterned metal pad.]

MARKED-UP VERSION SHOWING AMENDMENTS

24. (Amended) An etched optoelectronic apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;

b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls;

c) a patterned metal layer disposed directly on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls, and wherein the patterned metal layer includes a U-shaped patterned metal area, with the etched pit disposed inside the U-shaped patterned metal area; and

d) an optical component in the etched pit. [a patterned metal pad disposed on the dielectric layer;

e) solder disposed on the patterned metal pad.]

27. (Amended) An etched optoelectronic apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;

b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls;

c) a patterned metal layer disposed directly on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls;

d) a patterned metal pad disposed on the dielectric layer;

e) solder disposed on the patterned metal pad; and

f) an optoelectronic device on the solder.